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Box PATENT APPLICATION

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Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): IMMINK, Kees A. S.

For: METHOD AND APPARATUS FOR CODING INFORMATION, METHOD AND  
APPARATUS FOR DECODING INFORMATION, METHOD OF FABRICATING A  
RECORDING MEDIUM, THE RECORDING MEDIUM AND MODULATED SIGNAL

Enclosed are:

X A specification consisting of 30 pages

X 24 sheet(s) of Formal drawings

X An assignment of the invention

     Certified copy of Priority Document(s)

X Executed Declaration      Original X Photocopy

     A verified statement to establish small entity status under 37  
CFR 1.9 and 37 CFR 1.27

     Preliminary Amendment

     Information Disclosure Statement, PTO-1449 and reference(s)

Other

The filing fee has been calculated as shown below:

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INDEPENDENT	11 - 3 =	8	x80 =\$ 640.00	or	x 40 = \$ 0.00
MULTIPLE DEPENDENT CLAIM PRESENTED <u>no</u>			+270 = \$ 0.00	or	+135 = \$ 0.00
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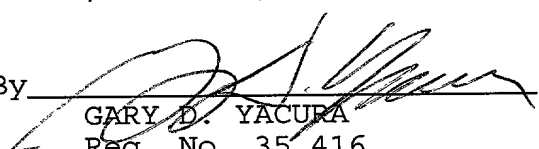
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Respectfully submitted,

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**METHOD AND APPARATUS FOR CODING INFORMATION,  
METHOD AND APPARATUS FOR DECODING CODED INFORMATION,  
METHOD OF FABRICATING A RECORDING MEDIUM,  
THE RECORDING MEDIUM AND MODULATED SIGNAL**

5

**FIELD OF THE INVENTION**

The present invention relates to coding information, and more particularly, to a method and apparatus for coding information having improved information density. The present invention further relates to producing a modulated signal from the coded information, producing a recording medium from the coded information, and the recording medium itself. The present invention still further relates to a method and apparatus for decoding coded information, and decoding coded information from a modulated signal and/or a recording medium.

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**BACKGROUND OF THE INVENTION**

When data is transmitted through a transmission line or recorded onto a recording medium such as a magnetic disc, an optical disc or a magneto-optical disc, the data is modulated into code matching the transmission line or the recording medium prior to the transmission or recording.

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Run length limited codes, generically designated as (d, k) codes, have been widely and successfully applied in modern magnetic and optical recording systems. Such codes, and means for implementing such codes are described by K. A. Schouhamer Immink in the book entitled "Codes for Mass Data Storage Systems" (ISBN 90-74249-23-X , 1999). Run length limited codes are extensions of earlier non return to zero recording codes, where binary recorded "zeros" are represented by no (magnetic flux) change in the recording medium, while binary "ones" are represented by transitions from one direction of recorded flux to the opposite direction.

25

In a (d, k) code, the above recording rules are maintained with the additional constraints that at least d "zeros" are recorded between successive "ones", and no more than k "zeros" are recorded between successive "ones". The

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first constraint arises to obviate intersymbol interference occurring because of pulse crowding of the reproduced transitions when a series of "ones" are contiguously recorded. The second constraint arises to ensure recovering a clock from the reproduced data by "locking" a phase locked loop to the reproduced transitions. If there is too long an unbroken string of contiguous "zeros" with no interspersed "ones", the clock regenerating phase-locked-loop will fall out of synchronism. In, for example, a (1,7) code there is at least one "zero" between recorded "ones", and there are no more than seven recorded contiguous "zeros" between recorded "ones".

The series of encoded bits is converted, via a modulo-2 integration operation, to a corresponding modulated signal formed by bit cells having a high or low signal value. A "one" bit is represented in the modulated signal by a change from a high to a low signal value or vice versa, and a "zero" bit is represented by the lack of change in the modulated signal.

The information conveying efficiency of such codes is typically expressed as a rate, which is the quotient of the number of bits ( $m$ ) in the information word to the number of bits ( $n$ ) in the code word (i.e.,  $m/n$ ). The theoretical maximum rate of a code, given values of  $d$  and  $k$ , is called the Shannon capacity. FIGURE 1 tabulates the Shannon capacity  $C(d,k)$  for  $d=1$  versus  $k$ . As shown, for a (1,7) code, the Shannon capacity,  $C(1,7)$ , has a value of 0.67929. This means that a (1,7) code cannot have a rate larger than 0.67929. The practical implementation of codes requires that the rate be a rational fraction, and to date the above (1,7) code has a rate  $2/3$ . This rate of  $2/3$  is slightly less than the Shannon capacity of 0.67929, and the code is therefore a highly efficient one. To achieve the  $2/3$  rate, 2 unconstrained data bits are mapped into 3 constrained encoded bits.

(1,7) codes having a rate of  $2/3$  and means for implementing associated encoders and decoders are known in the art. U.S. Patent No. 4,413,251 entitled "Method and Apparatus for Generating A Noiseless Sliding Block Code for a (1,7) Channel with Rate  $2/3$ ", issued in the names of Adler et al., discloses an encoder which is a finite-state machine having 5 internal states. U.S. Patent No. 4,488,142

entitled "Apparatus for Encoding Unconstrained Data onto a (1,7) Format with Rate 2/3", issued in the name of Franaszek discloses an encoder having 8 internal states.

However, a demand exists for even more efficient codes so that, for example, the information density on a recording medium or over a transmission line can be increased.

### SUMMARY OF THE INVENTION

In the converting method and apparatus according to the present invention, m-bit information words are converted into n-bit code words at a rate greater than 2/3. Consequently, the same amount of information can be recorded in less space, and information density increased.

In the present invention, n-bit code words are divided into a first type and a second type, and into coding states of a first kind and a second kind such that an m-bit information word is converted into an n-bit code word of the first or second kind if the previous m-bit information word was converted into an n-bit code word of the first type and is converted into an n-bit code word of the first kind if the previous m-bit information word was converted into an n-bit code word of the second type. In one embodiment, n-bit code words of the first type end in zero, n-bit code words of the second type end in one, n-bit code words of the first kind start with zero, and n-bit code words of the second kind start with zero or one. Furthermore, in the embodiments according to the present invention, the n-bit code words satisfy a dk-constraint of (1,k) such that a minimum of 1 zero and a maximum of k zeros falls between consecutive ones.

In other embodiments of the present invention, the coding device and method according to the present invention are employed to record information on a recording medium and create a recording medium according to the present invention.

In still other embodiments of the present invention, the coding device and method according to the present invention are further employed to transmit information.

In the decoding method and apparatus according to the present invention,  
 5 n-bit code words created according to the coding method and apparatus are decoded into m-bit information words. The decoding involves determining the state of a next n-bit code word, and based on the state determination, the current n-bit code word is converted into an m-bit information word.

In other embodiments of the present invention, the decoding device and  
 10 method according to the present invention are employed to reproduce information from a recording medium.

In still other embodiments of the present invention, the decoding device and method according to the present invention are employed to receive  
 15 information transmitted over a medium.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention will become more fully understood from the detailed description given herein below and the accompanying drawings which are given by way of illustration only, wherein like reference numerals designate  
 20 corresponding parts in the various drawings, and wherein:

FIGURE 1 tabulates the Shannon capacity  $C(d,k)$  for  $d=1$  versus  $k$ ;

FIGURE 2 shows an example of how the code words in the various subgroups are allocated in to the various states in the first embodiment;

FIGURE 3 shows an embodiment for a coding device according to the  
 25 invention;

FIGURES 4A-4H show a complete translation table according to the first embodiment for converting 9-bit information words into 13-bit code words;

FIGURE 5 illustrates the conversion of a series of information words into a series of code words using the translation table of FIGURES 4A-4H;

FIGURE 6 illustrates an embodiment of a recording device according to the present invention;

FIGURE 7 illustrates a recording medium and modulated signal according to the present invention;

5       FIGURE 8 illustrates a transmission device according to the present invention;

FIGURE 9 illustrates a decoding device according to the present invention;

FIGURE 10 illustrates a reproducing device according to the present invention;

10       FIGURE 11 illustrates a receiving device according to the present invention;

FIGURE 12 shows an example of how the code words in the various subgroups are allocated in to the various states in the second embodiment;

15       FIGURES 13A-13C show the beginning, middle and end portions of a translation table according to the second embodiment for converting 9-bit information words into 13-bit code words

FIGURE 14 shows an example of how the code words in the various subgroups are allocated in to the various states in the third embodiment;

20       FIGURES 15A-15C show the beginning, middle and end portions of a translation table according to the third embodiment for converting 11-bit information words into 16-bit code words

FIGURE 16 shows an example of how the code words in the various subgroups are allocated in to the various states in the fourth embodiment; and

25       FIGURES 17A-17C show the beginning, middle and end portions of a translation table according to the fourth embodiment for converting 13-bit information words into 19-bit code words.

#### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

30       The general coding method according to the present invention will be described followed by a specific first embodiment of the coding method. Next, the

general decoding method according to the present invention will be described in the context of the first embodiment. The various apparatuses according to the present invention will then be described. Specifically, the coding device, recording device, transmission device, decoding device, reproducing device and receiving  
5 device according to the present invention will be described. Afterwards, additional coding embodiments according to the present invention will be described.

#### CODING METHOD

According to the present invention, an m-bit information word is converted  
10 into an n-bit code word such that the rate of  $m/n$  is greater than  $2/3$ . The code words are divided into first and second types wherein the first type includes code words ending with "0" and the second type includes code words ending with "1." As a result, the code words of the first type are divided into two subgroups E00 and E10, and code words of the second type are divided into two subgroups E01  
15 and E11. Code word subgroup E00 includes code words that start with "0" and end with "0", code word subgroup E01 includes code words that start with "0" and end with "1", code word subgroup E10 includes code words that start with "1" and end with "0", and code word subgroup E11 includes code words that start with "1" and end with "1".

20 The code words are also divided into at least one state of a first kind and at least one state of a second kind. States of the first kind include code words that only start with "0," and states of the second kind include code words that start with either "0" or "1."

#### 25 CODING METHOD ACCORDING TO A FIRST EMBODIMENT

In a first preferred embodiment of the present invention, 9-bit information words are converted into 13-bit code words. The code words satisfy a (d,k) constraint of (1,k), and are divided into 3 states of the first kind and 2 states of the second kind (a total of 5 states). In order to reduce the k-constraint, three code  
30 words, namely, "0000000000000", "0000000000001", and "0000000000010" are



barred from the encoding tables. An enumeration of code words shows there are 231 code words in subgroup E00, 144 code words in subgroup E10, 143 code words in subgroup E01, and 89 code words in subgroup E11.

To perform encoding, each 13-bit code word in each state is associated with a coding state direction. The state direction indicates the next state from which to select a code word in the encoding process. The state directions are assigned to code words such that code words that end with a "0" (i.e. code words in subgroups E10 and E00) have associated state directions that indicate any of the  $r=5$  states, while code words that end with a "1" (i.e., code words in subgroups E01 and E11) have associated state directions that only indicate one of the states of the first kind. This ensures that the  $d=1$  constraint will be satisfied; namely, after a code word ending in "1", the next code word will start with "0".

Furthermore, while, as explained in more detail below, the same code word can be assigned to different information words in the same state, different states cannot include the same code word. In particular code words in subgroups E10 and E00 can be assigned 5 times to different information words within one state, while code words in subgroups E11 and E01 can be assigned 3 times to different information words within one state. As there are 231 code words in subgroup E00 and 144 code words in subgroup E10, there are 1875 ( $5 \times (231+144)$ ) "code word – state direction" combinations for code words of the first type. There are 143 code words in subgroup E01 and 89 code words in E11, so that there are 696 ( $3 \times (143+89)$ ) "code word – state direction" combinations for code words of the second type. In total  $1875+696=2571$  "code word - state direction" combinations exist.

For  $m$ -bit information words, there are a total of  $2^m$  possible information words. So, for 9-bit information words,  $2^9 = 512$  information words exist. Because there are five states in this encoding embodiment, 5 times  $512 = 2561$  of the "code word - state direction" combinations are needed. This leaves  $2571-2561 = 10$  remaining combinations.

The available code words in the various subgroups are distributed over the states of the first and second kind in compliance with the restrictions discussed above. FIGURE 2 shows an example of how the code words in the various subgroups are allocated in this embodiment to the various states. As shown in

5 FIGURE 2, in this example, states 1, 2, and 3 are states of the first kind and states 4 and 5 are states of the second kind. Taking the subgroup E00 of size 230 as an example, subgroup E00 has 76 code words in each of states 1, 2, and 3 plus 1 code word in each of states 4 and 5. And, taking state 1 as an example, in state 1 the number of “code word – state direction” combinations is  $5 \times 76 + 3 \times 44 = 512$ ,

10 which means that 9-bit information words can be assigned. Remember, each code word of the first type can be assigned any one of the five different states as a state directions, and therefore used five time within a state; while each code word of the second type can only be assigned one of the three states of the first kind as a state direction because of the  $d=1$  restriction, and therefore used three times

15 within a state.

It can be verified that from any of the  $r=5$  coding states shown in FIGURE 2 there at least 512 information words that can be assigned to code words, which is enough to accommodate 9-bit information words. In the manner described above any random series of 9-bit information words can be uniquely converted to a

20 series of code words.

FIGURES 4A-4H show a complete translation table according to this embodiment for converting 9-bit information words into 13-bit code words. Included in the translation table of FIGURES 4A-4H are the state direction assigned to each code word. Specifically, in FIGURES 4A-4H, the first column

25 shows the decimal notation of the information words in the second column. The third, fifth, seventh, ninth and eleventh columns show the code words (also referred to in the art as channel bits) assigned to the information words in states 1, 2, 3, 4 and 5, respectively. The fourth, sixth, eighth, tenth and twelfth columns show by way of the respective digits 1, 2, 3, 4 and 5 the state direction of the

associated code words in the third, fifth, seventh, ninth and eleventh columns, respectively.

The conversion of a series of information words into a series of code words will be further explained with reference to FIGURE 5. The first column of FIGURE 5 shows from top to bottom a series of successive 9-bit information words, and the second column shows in parenthesis the decimal values of these information words. The third column "state" is the coding state that is to be used for the conversion of the information word. The "state" is laid down when the preceding code word was delivered (i.e., the state direction of the preceding code word). The fourth column "code words" includes the code words assigned to the information words according to the translation table of FIGURES 4A-H. The fifth column "next state" is the state direction associated with the code word in the fourth column and is also determined according to the translation table of FIGURES 4A-H.

The first word from the series of information words shown in the first column of FIGURE 5 has a word value of "1" in decimal notation. Let us assume that the coding state is state 1 (S1) when the conversion of the series of information words is initiated. Therefore the first word is translated into code word "0000000000100" according to the state 1 set of code words from the translation table. At the same time the next state becomes state 2 (S2) because the state direction assigned to code word "0000000000100" representing decimal value 1 in state 1 is state 2. This means that the next information word (decimal value "3") is going to be translated using the code words in state 2. Consequently, the next information word, having a decimal value of "3", is translated into code word "0001010001010". Similar to the manner described above, the information words having the decimal values "5", "12" and "19" are converted.

#### DECODING METHOD

Hereinafter, decoding of n-bit code words (in this example 13-bit words) received from a recording medium will be further explained with reference to

FIGURES 4A-4H. For the purposes of description, assume that the word values of a series of successive code words received from, for example, a recording medium are "0000000000100", "0001010001010", "0101001001001". From the translation table of FIGURES 4A-4H, it is found that the first code word

5 "0000000000100" is assigned to the information words "0", "1", "2", "3" and "4" and state directions 1, 2, 3, 4 and 5, respectively. The next code word value is "0001010001010", and belongs to the set of code words in state 2. This means that the first code word "0000000000100" had a state direction of 2. The first code word "0000000000100" with a state direction of 2 represents the information word

10 having a decimal value of "1". Therefore, it is determined that the first code word represents information word "000000001" having a decimal value of "1".

Furthermore, the third code word "0101001001001" is a member of state 4. Therefore, it is determined in the same manner as above that the second code word "0001010001010" represents the information word having the decimal value

15 "3". In the same manner other code words can be decoded. It is noted that both the current code word and the next code words are observed to decode the current code word into a unique information word.

#### CODING DEVICE

20 FIGURE 3 shows an embodiment for a coding device 124 according to the invention. The coding device 124 converts m-bit information words into n-bit code words, where the number of different coding states r is represented by s bits. For example, when the number of coding states  $r = 5$ , s equals 3. As shown, the coding device 124 includes a converter 50 for converting (m+s) binary input

25 signals to (n+s) binary output signals. In a preferred embodiment, the converter 50 includes a read only memory (ROM) storing a translation table according to at least one embodiment of the present invention and address circuitry for addressing the translation table based on the m+s binary input signals. However, instead of a ROM, the converter 50 can include a combinatorial logic circuit

producing the same results as the translation table according to at least one embodiment of the present invention.

From the inputs of the converter 50, m inputs are connected to a first bus 51 for receiving m-bit information words. From the outputs of the converter 50, n  
5 outputs are connected to a second bus 52 for delivering n-bit code words. Furthermore, s inputs are connected to an s-bit third bus 53 for receiving a state word that indicates the instantaneous coding state. The state word is delivered by a buffer memory 54 including, for example, s flip-flops. The buffer memory 54 has s inputs connected to a fourth bus 55 for receiving a state direction to be loaded  
10 into the buffer memory 54 as the state word. For delivering the state directions to be loaded in the buffer memory 54, the s outputs of the converter 50 are used.

The second bus 52 is connected to the parallel inputs of a parallel-to-serial converter 56, which converts the code words received over the second bus 52 to a serial bit string. A signal line 57 supplies the serial bit string to a modulator  
15 circuit 58, which converts the bit string into a modulated signal. The modulated signal is then delivered over a line 60. The modulator circuit 58 is any well-known circuit for converting binary data into a modulated signal such as a modula-2 integrator.

For the purposes of synchronizing the operation of the coding device, the  
20 coding device includes a clock generating circuit (not shown) of a customary type for generating clock signals for controlling timing of, for example, the parallel/serial converter 58 and the loading of the buffer memory 54.

In operation, the converter 50 receives m-bit information words and an s-bit state word from the first bus 51 and the third bus 53, respectively. The s-bit state  
25 word indicates the state in the translation table to use in converting the m-bit information word. Accordingly, based on the value of the m-bit information word, the n-bit code word is determined from the code words in the state identified by the s-bit state word. Also, the state direction associated with the n-bit code word is determined. The state direction, namely, the value thereof is converted into an s-  
30 bit binary word; or alternatively, the state directions are stored in the translation

table as s-bit binary words. The converter 50 outputs the n-bit code word on the second bus 52, and outputs the s-bit state direction on fourth bus 55. The buffer memory 54 stores the s-bit state direction as a state word, and supplies the s-bit state word to the converter 50 over the third bus 53 in synchronization with the receipt of the next m-bit information word by the converter 50. This synchronization is produced based on the clock signals discussed above in any well-known manner.

The n-bit code words on the second bus 52 are converted to serial data by the parallel/serial converter 56, and then the serial data is converted into a modulated signal by the modulator 58.

The modulated signal may then undergo further processing for recordation or transmission.

#### RECORDING DEVICE

FIGURE 6 shows a recording device for recording information that includes the coding device 124 according to the present invention as shown in FIGURE 3. As shown in FIGURE 6, m-bit information is converted into a modulated signal through the coding device 124. The modulated signal produced by the coding device 124 is delivered to a control circuit 123. The control circuit 123 may be any conventional control circuit for controlling an optical pick-up or laser diode 122 in response to the modulated signal applied to the control circuit 123 so that a pattern of marks corresponding to the modulated signal are recorded on the recording medium 110.

FIGURE 7 shows by way of example, a recording medium 110 according to the invention. The recording medium 110 shown is a read-only memory (ROM) type optical disc. However, the recording medium 110 of the present invention is not limited to a ROM type optical disk, but could be any type of optical disk such as a write-once read-many (WORM) optical disk, random accessible memory (RAM) optical disk, etc. Further, the recording medium 110 is not limited to being

an optical disk, but could be any type of recording medium such as a magnetic disk, a magneto-optical disk, a memory card, magnetic tape, etc.

As shown in FIGURE 7, the recording medium 110 according to one embodiment of the present invention includes information patterns arranged in tracks 111. Specifically, FIGURE 7 shows an enlarged view of a track 111 along a direction 114 of the track 111. As shown, the track 111 includes pit regions 112 and non-pit regions 113. Generally, the pit and non-pit regions 112 and 113 represent constant signal regions of the modulated signal 115 (zeros in the code words) and the transitions between pit and non-pit regions represent logic state transitions in the modulated signal 115 (ones in the code words).

As discussed above, the recording medium 110 may be obtained by first generating the modulated signal and then recording the modulated signal on the recording medium 110. Alternatively, if the recording medium is an optical disc, the recording medium 110 can also be obtained with well-known mastering and replica techniques.

#### TRANSMISSION DEVICE

FIGURE 8 shows a transmission device for transmitting information that includes the coding device 124 according to the present invention as shown in FIGURE 3. As shown in FIGURE 8, m-bit information words are converted into a modulated signal through the coding device 124. A transmitter 150 then further processes the modulated signal, to convert the modulated signal into a form for transmission depending on the communication system to which the transmitter belongs, and transmits the converted modulated signal over a transmission medium such as air (or space), optical fiber, cable, a conductor, etc.

#### DECODING DEVICE

FIGURE 9 illustrates a decoder according to the present invention. The decoder performs the reverse process of the converter of FIGURE 3 and converts n-bit code words of the present invention into m-bit information words. As shown,

the decoder 100 includes a first look-up table (LUT) 102 and a second LUT 104. The first and second LUTs 102 and 104 store the translation table used to create the n-bit code words being decoded. Where K refers to time, the first LUT 102 receives the (K+1)th n-bit code word and the second LUT 104 receives the output of the first LUT 102 and the Kth n-bit code word. Accordingly, the decoder 100 operates as a sliding block decoder. At every block time instant the decoder 100 decodes one n-bit code word into one m-bit information word and proceeds with the next n-bit code word in the serial data (also referred to as the channel bit stream).

10 In operation, the first LUT 102 determines the state of the (K+1)th code word from the stored translation table, and outputs the state to the second LUT 104. So the output of the first LUT 102 is a binary number in the range of 1, 2, ..., r (where r denotes the number of states in the translation table). The second LUT 104 determines the possible m-bit information words associated with Kth code word from the Kth code word using the stored translation table, and then determines the specific one of the possible m-bit information words being represented by the n-bit code word using the state information from the first LUT 102 and the stored translation table.

For the purposes of further explanation only, assume the n-bit code words are 13-bit code words produced using the translation table of FIGURES 4A-4H. Then, referring to FIGURE 5, if the (K+1)th 13-bit code word is "0001010001010" the first LUT 102 determines the state as state 2. Furthermore, if the Kth 13-bit code word is "0000000000100", then the second LUT 104 determines that the Kth 13-bit code word represents one of the 9-bit information words having a decimal value of 0, 1, 2, 3 or 4. And, because the next state or state direction of state 2 is supplied by the first LUT 102, the second LUT 104 determines that the Kth 13-bit code word represents the 9-bit information word having a decimal value of 1 because the 13-bit code word "0000000000100" associated with a state direction of 2 represents the 9-bit information word having a decimal value of 1.

30



## REPRODUCING DEVICE

FIGURE 10 illustrates a reproducing device that includes the decoder 100 according to the present invention as shown in FIGURE 9. As shown, the reading device includes an optical pick-up 122 of a conventional type for reading a recording medium 110 according to the invention. The recording medium 110 may be any type of recording medium such as discussed previously. The optical pick-up 122 produces an analog read signal modulated according to the information pattern on the recording medium 110. A detection circuit 125 converts this read signal in conventional fashion into a binary signal of the form acceptable to the decoder 100. The decoder 100 decodes the binary signal to obtain the m-bit information words.

## RECEIVING DEVICE

FIGURE 11 illustrates a receiving device that includes the decoder 100 according to the present invention as shown in FIGURE 9. As shown, the receiving device includes a receiver 160 for receiving a signal transmitted over a medium such as air (or space), optical fiber, cable, a conductor, etc. The receiver 160 converts the received signal into a binary signal of the form acceptable to the decoder 100. The decoder 100 decodes the binary signal to obtain the m-bit information words.

## CODING METHOD ACCORDING TO A SECOND EMBODIMENT

FIGURES 12 and 13A-13C illustrate another embodiment of the present invention. According to this embodiment, the greater than  $2/3$  rate is achieved by converting 9-bit information words into 13-bit code words; wherein the number of coding states  $r$  equals 13, and 8 of the coding states are coding states of the first kind and 5 of the coding states are coding states of the second kind. Also, the code words satisfy a  $(d,k)$  constraint of  $(1,k)$ . FIGURE 12 corresponds to FIGURE 2 of the first embodiment, and illustrates the division of code words among the states in this second embodiment.

As described above, code words that end with a "0", i.e. code words in subgroups E00 and E10, are allowed to enter any of the  $r=13$  states, while code words that end with a "1" i.e. code words in subgroups E01 and E11, may only enter the states of the first kind(State 1 to State 8).

5 Therefore, code words in subgroups E00 and E10 can be assigned 13 times to different information words, while code words in subgroups E01 and E11 can be assigned 8 times to different information words. Referring to FIGURE 12, subgroup E00 has 24 code words in state 1 and the subgroup E01 has 25 code words in state 1. So the number of "code words - state direction" combinations is  
 10  $(13 \times 24) + (8 \times 25) = 512$ , which means that 9-bit information words can be assigned. It can be verified that from any of the  $r=13$  coding states there at least 512 information words that can be assigned to code words, which is enough to accommodate 9-bit information words.

FIGURES 13A-13C illustrate the beginning, middle and end portions of the  
 15 translation table for this second embodiment in the same fashion that FIGURES 4A-4H illustrated the translation table for the first embodiment.

#### CODING METHOD ACCORDING TO A THIRD EMBODIMENT

FIGURES 14 and 15A-15C illustrate another embodiment of the present  
 20 invention. According to this embodiment, the greater than  $2/3$  rate is achieved by converting 11-bit information words into 16-bit code words; wherein the number of coding states  $r$  equals 13, and 8 of the coding states are coding states of the first kind and 5 of the coding states are coding states of the second kind. Also, the code words satisfy a  $(d,k)$  constraint of  $(1,k)$ . FIGURE 14 corresponds to FIGURE  
 25 2 of the first embodiment, and illustrates the division of code words among the states in this third embodiment. It can be verified that from any of the  $r=13$  coding states there at least 2048 information words that can be assigned to code words, which is enough to accommodate 11-bit information words.

FIGURES 15A-15C illustrate the beginning, middle and end portions of the translation table for the third embodiment in the same fashion that FIGURES 4A-4H illustrated the translation table for the first embodiment.

5            CODING METHOD ACCORDING TO A FOURTH EMBODIMENT

FIGURES 16 and 17A-17C illustrate another embodiment of the present invention. According to this embodiment, the greater than  $2/3$  rate is achieved by converting 13-bit information words into 19-bit code words; wherein the number of coding states  $r$  equals 5, and 3 of the coding states are coding states of the first kind and 2 of the coding states are coding states of the second kind. Also, the code words satisfy a  $(d,k)$  constraint of  $(1,k)$ . FIGURE 16 corresponds to FIGURE 2 of the first embodiment, and illustrates the division of code words among the states in this fourth embodiment. It can be verified that from any of the  $r=5$  coding states there at least 8192 information words that can be assigned to code words, which is enough to accommodate 13-bit information words.

FIGURES 17A-17C illustrate the beginning, middle and end portions the translation table for the fourth embodiment in the same fashion that FIGURES 4A-4H illustrated the translation table for the first embodiment.

The invention has been described in detail with particular reference to preferred embodiments thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

I Claim:

1. A method of converting, comprising:

receiving m-bit information words, where m is an integer;

converting the m-bit information words into n-bit code words, where n is an integer greater than m, the n-bit code words being divided into a first type and a second type and into coding states of a first kind and a second kind such that an m-bit information word is converted into an n-bit code word of the first or second kind if the previous m-bit information word was converted into an n-bit code word of the first type and is converted into an n-bit code word of the first kind if the previous m-bit information word was converted into an n-bit code word of the second type.

2. The method of claim 1, wherein the converting step converts the m-bit information words into n-bit code words that satisfy a dk-constraint, where d indicates a minimum number of zeros between consecutive ones in the n-bit code words and k indicates a maximum number of zeros between consecutive ones in the n-bit code words.

3. The method of claim 2, wherein  $m/n$  is greater than  $2/3$ , and  $d = 1$ .

4. The method of claim 2, wherein  $d = 1$ .

5. The method of claim 2, wherein the n-bit code words are divided into p coding states of the first kind and q coding states of the second kind, where p and q are integers greater than or equal to 1, and each of the p and q coding states have n-bit code words different from the n-bit code words in the other p and q coding states.

6. The method of claim 5, wherein  $m/n$  is greater than  $2/3$ ,  $d = 1$ ,  $p = 3$  and  $q = 2$ .

7. The method of claim 5, wherein  $p = 3$  and  $q = 2$ .
8. The method of claim 5, wherein  $p+q$  equals 5.
9. The method of claim 5, wherein  $m/n$  is greater than  $2/3$ ,  $d = 1$ ,  $p = 8$  and  $q = 5$ .
10. The method of claim 5, wherein  $p = 8$  and  $q = 5$ .
11. The method of claim 5, wherein  $p+q$  equals 13.
12. The method of claim 5, wherein at least one of the  $n$ -bit code words in one of the  $p$  coding states is associated with  $p+q$  of the  $m$ -bit information words.
13. The method of claim 12, wherein at least one of the  $n$ -bit code words in one of the  $q$  coding states is associated with  $p$  of the  $m$ -bit information words.
14. The method of claim 5, wherein at least one of the  $n$ -bit code words in one of the  $q$  coding states is associated with  $p$  of the  $m$ -bit information words.
15. The method of claim 1, wherein the  $n$ -bit code words are divided into  $p$  coding states of the first kind and  $q$  coding states of the second kind, where  $p$  and  $q$  are integers greater than or equal to 1, and each of the  $p$  and  $q$  coding states have  $n$ -bit code words different from the  $n$ -bit code words in the other  $p$  and  $q$  coding states.
16. The method of claim 15, wherein  $p+q$  equals 5.
17. The method of claim 15, wherein  $p+q$  equals 13.

18. The method of claim 15, wherein at least one of the  $n$ -bit code words in one of the  $p$  coding states is associated with  $p+q$  of the  $m$ -bit information words.

19. The method of claim 18, wherein at least one of the  $n$ -bit code words in one of the  $q$  coding states is associated with  $p$  of the  $m$ -bit information words.

20. The method of claim 15, wherein at least one of the  $n$ -bit code words in one of the  $q$  coding states is associated with  $p$  of the  $m$ -bit information words.

21. The method of claim 1, wherein the  $n$ -bit code words of the first type end in zero, the  $n$ -bit code words of the second type end in one, the  $n$ -bit code words in a coding state of the first kind start with zero, and the  $n$ -bit code words in a coding state of the second kind start with zero or one.

22. The method of claim 1, wherein the  $n$ -bit code words of the first type end in zero, and the  $n$ -bit code words of the second type end in one.

23. The method of claim 1, wherein the  $n$ -bit code words in a coding state of the first kind start with zero, and the  $n$ -bit code words in a coding state of the second kind start with zero or one.

24. The method of claim 1, wherein the converting step converts at a coding rate of  $m/n$ , which is greater than  $2/3$ .

25. The method of claim 24, wherein  $n$  is equal one of 13, 16, and 19.

26. The method of claim 24, wherein  $m$  is equal to one of 9, 11, and 13.

27. The method of claim 1, further comprising:

generating a modulated signal from the  $n$ -bit code words.

28. The method of claim 27, further comprising:  
recording the modulated signal in a recording medium.
- 5 29. The method of claim 27, further comprising:  
transmitting the modulated signal.
30. The method of claim 1, wherein the converting step converts the m-bit  
information words into the n-bit code words using a translation table.
- 10 31. A method of converting, comprising:  
receiving m-bit information words, where m is an integer;  
converting the m-bit information words into n-bit code words, where n is an  
integer greater than m, at a coding rate  $m/n$  greater than  $2/3$ .
- 15 32. A method of converting, comprising:  
receiving m-bit information words, where m is an integer;  
converting the m-bit information words into n-bit code words that satisfy a  
dk-constraint, where n is an integer greater than m, d indicates a minimum  
20 number of zeros between consecutive ones in the n-bit code words and k  
indicates a maximum number of zeros between consecutive ones in the n-bit code  
words, the n-bit code words being divided into a first type and a second type and  
into coding states of a first kind and a second kind such that an m-bit information  
word is converted into an n-bit code word of the first or second kind if the previous  
25 m-bit information word was converted into an n-bit code word of the first type and  
is converted into an n-bit code word of the first kind if the previous m-bit  
information word was converted into an n-bit code word of the second type, the n-  
bit code words of the first type ending in zero, the n-bit code words of the second  
type ending in one, the n-bit code words in a coding state of the first kind starting  
30 with zero and the n-bit code words in a coding state of the second kind starting

with zero or one, and the n-bit code words being divided into p coding states of the first kind and q coding states of the second kind, where p and q are integers greater than or equal to 1, and each of the p and q coding states have n-bit code words different from the n-bit code words in the other p and q coding states.

5

33. A coding device, comprising:

a converter receiving m-bit information words, where m is an integer and converting the m-bit information words into n-bit code words, where n is an integer greater than m, the n-bit code words being divided into a first type and a second type and into coding states of a first kind and a second kind such that an m-bit information word is converted into an n-bit code word of the first or second kind if the previous m-bit information word was converted into an n-bit code word of the first type and is converted into an n-bit code word of the first kind if the previous m-bit information word was converted into an n-bit code word of the second type.

15

34. The coding device of claim 33, wherein the converter receives a coding state with each m-bit information word and converts the m-bit information word into the n-bit code word based on the coding state.

20

35. The coding device of claim 34, further comprising:

a buffer supplying the coding state to the converter; and wherein the converter determines the coding state for the next m-bit information word as part of the converting process, and stores the determined coding state in the buffer.

25

36. The coding device of claim 35, wherein the converter converts the m-bit information word into the n-bit code word and determines the coding state using a translation table.

30

37. The coding device of claim 33, further comprising:



a modulator generating a modulated signal from the n-bit code words.

38. The coding device of claim 37, further comprising:

a recording device recording the modulated signal in a recording medium.

5

39. The coding device of claim 37, further comprising:

a transmitter transmitting the modulated signal.

10 40. A method of manufacturing a recording medium, comprising:

converting m-bit information words into n-bit code words, where n is an integer greater than m, the n-bit code words being divided into a first type and a second type and into coding states of a first kind and a second kind such that an m-bit information word is converted into an n-bit code word of the first or second  
15 kind if the previous m-bit information word was converted into an n-bit code word of the first type and is converted into an n-bit code word of the first kind if the previous m-bit information word was converted into an n-bit code word of the second type;

generating a modulated signal from the n-bit code words; and

20 recording the modulated signal in a recording medium.

41. A recording medium having a modulated signal recorded in a track, the modulated signal including signal portions representing n-bit code words, where n is an integer, each n-bit code word representing an m-bit information word, where  
25 m is an integer less than n, the n-bit code words being divided into a first type and a second type and into coding states of a first kind and a second kind such that an m-bit information word is represented by an n-bit code word of the first or second kind if the previous m-bit information word is represented by an n-bit code word of the first type and is represented by an n-bit code word of the first kind if the

previous m-bit information word is represented by an n-bit code word of the second type.

42. The recording medium of claim 41, wherein the signal portions represent the  
5 n-bit code words such that each successive n-bit code word partially instructs a reproducing device on which of at least two m-bit information words are represented by each previous n-bit code word.

43. A modulated signal, comprising:  
10 signal portions representing n-bit code words, where n is an integer, each n-bit code word representing an m-bit information word, where m is an integer less than n, the n-bit code words being divided into a first type and a second type and into coding states of a first kind and a second kind such that an m-bit information  
15 word is represented by an n-bit code word of the first or second kind if the previous m-bit information word is represented by an n-bit code word of the first type and is represented by an n-bit code word of the first kind if the previous m-bit information word is represented by an n-bit code word of the second type.

44. The modulated signal of claim 43, wherein the signal portions represent the n-  
20 bit code words such that each successive n-bit code word partially instructs a reproducing device on which of at least two m-bit information words are represented by each previous n-bit code word.

45. A method of decoding, comprising:  
25 receiving n-bit code words, where n is an integer;  
converting the n-bit code words into m-bit information words, where m is an integer less than n, the n-bit code words being divided into a first type and a second type and into coding states of a first kind and a second kind such that an m-bit information word is represented by an n-bit code word of the first or second

kind if the previous n-bit code word is of the first type and is represented by an n-bit code word of the first kind if the previous n-bit code word is of the second type.

46. The method of claim 45, wherein the n-bit code words are divided into p coding states of the first kind and q coding states of the second kind, where p and q are integers greater than or equal to 1, and each of the p and q coding states have n-bit code words different from the n-bit code words in the other p and q coding states.
47. The method of claim 46, wherein the converting step determines to which of the p and q coding states a next n-bit code word belongs, and converts a current n-bit code word into an m-bit information word based on the determined coding state.
48. The method of claim 47, wherein at least one of the p and q coding states includes more than one of a same n-bit code word, the same n-bit code word maps to more than one of the m-bit information words, and each same n-bit code word has a different state direction associated therewith, each state direction indicating a next one of the p and q coding states from which to obtain the next n-bit code word when converting the m-bit information words into the n-bit code words.
49. The method of claim 48, wherein the n-bit code words satisfy a dk-constraint, where d indicates a minimum number of zeros between consecutive ones in the n-bit code words and k indicates a maximum number of zeros between consecutive ones in the n-bit code words.
50. The method of claim 49, wherein  $m/n$  is greater than  $2/3$ , and  $d = 1$ .
51. The method of claim 50, wherein  $p+q$  equals 5.

52. The method of claim 50, wherein  $p+q$  equals 13.

53. The method of claim 49, wherein the  $n$ -bit code words of the first type end in zero, the  $n$ -bit code words of the second type end in one, the  $n$ -bit code words in a coding state of the first kind start with zero, and the  $n$ -bit code words in a coding state of the second kind start with zero or one.

54. The method of claim 45, further comprising:

10       receiving a modulated signal; and  
           demodulating the modulated signal into at least the  $n$ -bit code words.

55. The method of claim 45, further comprising:

15       reproducing a modulated signal from a recording medium; and  
           demodulating the modulated signal into at least the  $n$ -bit code words.

56. A method of decoding, comprising:

20       receiving  $n$ -bit code words, where  $n$  is an integer;  
           determining a coding state of a next  $n$ -bit code word; and  
           converting a current  $n$ -bit code word into an  $m$ -bit information word, where  $m$  is an integer less than  $n$ , based on the determined coding state.

57. The method of claim 56, wherein each  $n$ -bit code word belongs to a coding state, at least one of the coding states includes more than one of a same  $n$ -bit code word, the same  $n$ -bit code word maps to more than one of the  $m$ -bit information words, and each same  $n$ -bit code word has a different state direction associated therewith, each state direction indicating a next one of the coding states from which to obtain the next  $n$ -bit code word when converting the  $m$ -bit information words into the  $n$ -bit code words.

30

58. The method of claim 56, further comprising:

receiving a modulated signal; and

demodulating the modulated signal into at least the n-bit code words.

5 59. The method of claim 56, further comprising:

reproducing a modulated signal from a recording medium; and

demodulating the modulated signal into at least the n-bit code words.

60. A decoding device, comprising:

10 a converter receiving n-bit code words, where n is an integer, and  
converting the n-bit code words into m-bit information words, where m is an  
integer less than n, the n-bit code words being divided into a first type and a  
second type and into coding states of a first kind and a second kind such that an  
m-bit information word is represented by an n-bit code word of the first or second  
15 kind if the previous n-bit code word is of the first type and is represented by an n-  
bit code word of the first kind if the previous n-bit code word is of the second type.

61. The decoding device of claim 60, wherein the n-bit code words are divided into  
p coding states of the first kind and q coding states of the second kind, where p  
20 and q are integers greater than or equal to 1, and each of the p and q coding  
states have n-bit code words different from the n-bit code words in the other p and  
q coding states.

62. The decoding device of claim 61, wherein the converter determines to which  
25 of the p and q coding states a next n-bit code word belongs, and converts a  
current n-bit code word into an m-bit information word based on the determined  
coding state.

63. The decoding device of claim 62, wherein at least one of the p and q coding  
30 states includes more than one of a same n-bit code word, the same n-bit code

word maps to more than one of the m-bit information words, and each same n-bit code word has a different state direction associated therewith, each state direction indicating a next one of the p and q coding states from which to obtain the next n-bit code word when converting the m-bit information words into the n-bit code words.

64. The decoding device of claim 63, wherein the n-bit code words satisfy a dk-constraint, where d indicates a minimum number of zeros between consecutive ones in the n-bit code words and k indicates a maximum number of zeros between consecutive ones in the n-bit code words.

65. The decoding device of claim 64, wherein  $m/n$  is greater than  $2/3$ , and  $d = 1$ .

66. The decoding device of claim 65, wherein  $p+q$  equals 5.

67. The decoding device of claim 65, wherein  $p+q$  equals 13.

68. The decoding device of claim 64, wherein the n-bit code words of the first type end in zero, the n-bit code words of the second type end in one, the n-bit code words in a coding state of the first kind start with zero, and the n-bit code words in a coding state of the second kind start with zero or one.

69. The decoding device of claim 60, further comprising:

a demodulator receiving a modulated signal and demodulating the modulated signal into at least the n-bit code words.

70. The decoding device of claim 60, further comprising:

a reproducing device reproducing a modulated signal from a recording medium, and demodulating the modulated signal into at least the n-bit code words.

71. A decoding device, comprising:

a first translator receiving a next  $n$ -bit code words, where  $n$  is an integer, and determining a coding state of the next  $n$ -bit code word;

5 a second translator receiving a current  $n$ -bit code word and the determined coding state, and converting the current  $n$ -bit code word into an  $m$ -bit information word, where  $m$  is an integer less than  $n$ , based on the determined coding state.

72. The decoding device of claim 71, wherein each  $n$ -bit code word belongs to a coding state, at least one of the coding states includes more than one of a same  $n$ -bit code word, the same  $n$ -bit code word maps to more than one of the  $m$ -bit information words, and each same  $n$ -bit code word has a different state direction associated therewith, each state direction indicating a next one of the coding states from which to obtain the next  $n$ -bit code word when converting the  $m$ -bit information words into the  $n$ -bit code words.

73. The decoding device of claim 71, further comprising:

a demodulator receiving a modulated signal and demodulating the modulated signal into at least the  $n$ -bit code words.

74. The decoding device of claim 71, further comprising:

a reproducing device reproducing a modulated signal from a recording medium, and demodulating the modulated signal into at least the  $n$ -bit code words.

**ABSTRACT OF THE DISCLOSURE**

In the coding device and method, m-bit information words are converted into n-bit code words such that the coding rate  $m/n$  is greater than  $2/3$ . The n-bit code words are divided into a first type and a second type, and into coding states of a first kind and a second kind such that an m-bit information word is converted into an n-bit code word of the first or second kind if the previous m-bit information word was converted into an n-bit code word of the first type and is converted into an n-bit code word of the first kind if the previous m-bit information word was converted into an n-bit code word of the second type. In one embodiment, n-bit code words of the first type end in zero, n-bit code words of the second type end in one, n-bit code words of the first kind start with zero, and n-bit code words of the second kind start with zero or one. Furthermore, in the embodiments, the n-bit code words satisfy a dk-constraint of (1,k) such that a minimum of 1 zero and a maximum of k zeros falls between consecutive ones. The coding device and method are employed to record information on a recording medium and thus create the recording medium. The coding device and method are further employed to transmit information. In the decoding method and apparatus, n-bit code words are decoded into m-bit information words. The decoding involves determining the state of a next n-bit code word, and based on the state determination, the current n-bit code word is converted into an m-bit information word. The decoding device and method are employed to reproduce information from a recording medium, and to receive information transmitted over a medium.



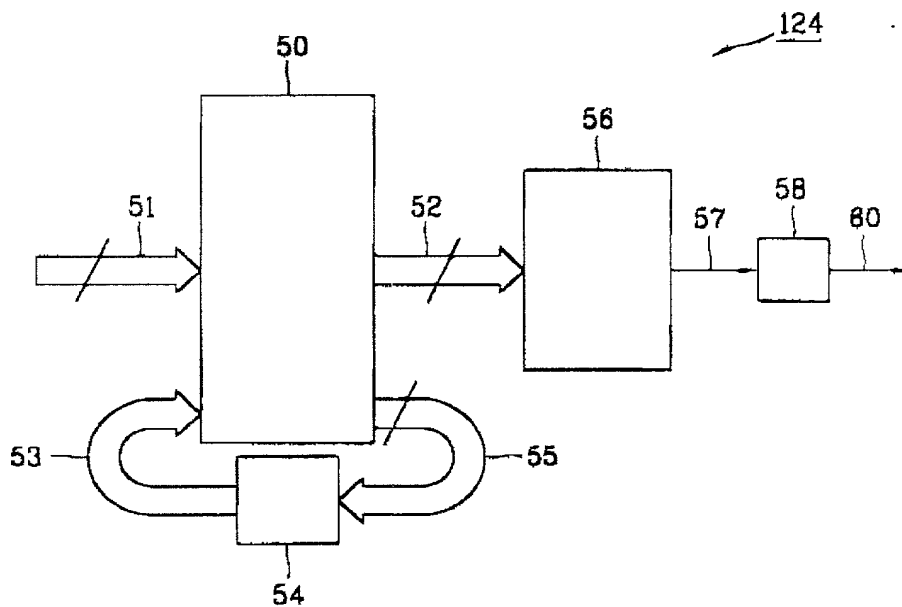
FIG. 1  
BACKGROUND ART

k	C(1,k)
7	0.67929
8	0.68525
9	0.68879
INF.	0.69424

FIG. 2

	1st KIND			2nd KIND	
SUBGROUP	STATE 1	STATE 2	STATE 3	STATE 4	STATE 5
E00	76	76	76	1	1
E01	44	44	44	5	6
E10	0	0	0	72	71
E11	0	0	0	44	45

FIG. 3



State 1		State 2		State 3		State 4		State 5		
Data bits	Channel bits	state	Channel bits	state	Channel bits	state	Channel bits	state	Channel bits	
0 00000000	0000000000100	1	0001010001010	1	0101000000100	1	0101000000000	1	1010101010101	3
1 00000001	0000000000100	2	0001010001010	2	0101000000100	2	0101000000000	2	0010000000000	2
2 00000010	0000000000100	3	0001010001010	3	0101000000100	3	0101000000000	3	0010000000000	3
3 00000011	0000000000100	4	0001010001010	4	0101000000100	4	0101000000000	4	0010000000000	4
4 00000100	0000000000100	5	0001010001010	5	0101000000100	5	0101000000000	5	0010000000000	5
5 00000101	0000000000100	1	0001010001010	1	0100000100100	1	0101000100100	1	0101010001001	1
6 00000110	0000000000100	2	0001010001010	2	0100000100100	2	0101000100100	2	0101010001001	2
7 00000111	0000000000100	3	0001010001010	3	0100000100100	3	0101000100100	3	0101010001001	3
8 00001000	0000000000100	4	0001010001010	4	0100000100100	4	0101000100100	4	0101010001001	4
9 00001001	0000000000100	5	0001010001010	5	0100000100100	5	0101000100100	5	0101010001001	5
10 00001010	0000000000101	1	0001010001010	1	0101000000100	1	0101000000100	1	0101010001001	1
11 00001011	0000000000101	2	0001010001010	2	0101000000100	2	0101000000100	2	0101010001001	2
12 00001100	0000000000101	3	0001010001010	3	0101000000100	3	0101000000100	3	0101010001001	3
13 00001101	0000000000101	4	0001010001010	4	0101000000100	4	0101000000100	4	0101010001001	4
14 00001110	0000000000101	5	0001010001010	5	0101000000100	5	0101000000100	5	0101010001001	5
15 00001111	0000000000100	1	0001010001010	1	0101000000100	1	0101000000100	1	0101010001001	1
16 00010000	0000000000100	2	0001010001010	2	0101000000100	2	0101000000100	2	0101010001001	2
17 00010001	0000000000100	3	0001010001010	3	0101000000100	3	0101000000100	3	0101010001001	3
18 00010010	0000000000100	4	0001010001010	4	0101000000100	4	0101000000100	4	0101010001001	4
19 00010011	0000000000100	5	0001010001010	5	0101000000100	5	0101000000100	5	0101010001001	5
20 00010100	0000000000101	1	0000000000000	1	0000000000000	1	0000000000000	1	0101010001001	1
21 00010101	0000000000101	2	0000000000000	2	0000000000000	2	0000000000000	2	0101010001001	2
22 00010110	0000000000101	3	0000000000000	3	0000000000000	3	0000000000000	3	0101010001001	3
23 00010111	0000000000101	4	0000000000000	4	0000000000000	4	0000000000000	4	0101010001001	4
24 00011000	0000000000101	5	0000000000000	5	0000000000000	5	0000000000000	5	0101010001001	5
25 00011001	0000000000101	1	0000000000000	1	0101000100100	1	0000000000100	1	0101010001001	1
26 00011010	0000000000101	2	0000000000000	2	0101000100100	2	0000000000100	2	0101010001001	2
27 00011011	0000000000101	3	0000000000000	3	0101000100100	3	0000000000100	3	0101010001001	

FIG. 4B

Data bits	Channel bits	state	Channel bits	state	Channel bits	state	Channel bits	state
64 001000000	0000001000010	5	0010010000010	5	0001010000100	5	1000010000010	5
65 001000001	0000001000100	1	0010010000100	1	0101010000100	1	1000010000100	1
66 001000010	0000001000100	2	0010010000100	2	0101010000100	2	1000010000100	2
67 001000011	0000001000100	3	0010010000100	3	0101010000100	3	1000010000100	3
68 001000100	0000001000100	4	0010010000100	4	0101010000100	4	1000010000100	4
69 001000101	0000001000100	5	0010010000100	5	0101010000100	5	1000010000100	5
70 001000110	0000001000100	1	0010010000100	1	0100010000100	1	1000010000100	1
71 001000111	0000001000100	2	0010010000100	2	0100010000100	2	1000010000100	2
72 001001000	0000001000100	3	0010010000100	3	0100010000100	3	1000010000100	3
73 001001001	0000001000100	4	0010010000100	4	0100010000100	4	1000010000100	4
74 001001010	0000001000100	5	0010010000100	5	0100010000100	5	1000010000100	5
75 001001011	0000001000100	1	0010010000100	1	0100010000100	1	1000010000100	1
76 001001100	0000001000100	2	0010010000100	2	0100010000100	2	1000010000100	2
77 001001101	0000001000100	3	0010010000100	3	0100010000100	3	1000010000100	3
78 001001110	0000001000100	4	0010010000100	4	0100010000100	4	1000010000100	4
79 001001111	0000001000100	5	0010010000100	5	0100010000100	5	1000010000100	5
80 001010000	0000001000100	1	0010010000100	1	0101010000100	1	1000010000100	1
81 001010001	0000001000100	2	0010010000100	2	0101010000100	2	1000010000100	2
82 001010010	0000001000100	3	0010010000100	3	0101010000100	3	1000010000100	3
83 001010011	0000001000100	4	0010010000100	4	0101010000100	4	1000010000100	4
84 001010100	0000001000100	5	0010010000100	5	0101010000100	5	1000010000100	5
85 001010101	0000001000100	1	0010010000100	1	0101010000100	1	1000010000100	1
86 001010110	0000001000100	2	0010010000100	2	0101010000100	2	1000010000100	2
87 001010111	0000001000100	3	0010010000100	3	0101010000100	3	1000010000100	3
88 001011000	0000001000100	4	0010010000100	4	0101010000100	4	1000010000100	4
89 001011001	0000001000100	5	0010010000100	5	0101010000100	5	1000010000100	5
90 001011010	0000001000100	1	0010010000100	1	0101010000100	1	1000010000100	1
91 001011011	0000001000100	2	0010010000100	2	0101010000100	2	1000010000100	2
92 001011100	0000001000100	3	0010010000100	3	0101010000100	3	1000010000100	3
93 001011101	0000001000100	4	0010010000100	4	0101010000100	4	1000010000100	4
94 001011110	0000001000100	5	0010010000100	5	0101010000100	5	1000010000100	5
95 001011111	0000001000100	1	0010010000100	1	0101010000100	1	1000010000100	1
96 001100000	0000010000000	2	0010100010010	2	0100010000100	2	1000100010010	2
97 001100001	0000010000000	3	0010100010010	3	0100010000100	3	1000100010010	3
98 001100010	0000010000000	4	0010100010010	4	0100010000100	4	1000100010010	4
99 001100011	0000010000000	5	0010100010010	5	0100010000100	5	1000100010010	5
100 001100100	0000010000000	1	0010100010010	1	0100010000100	1	1000100010010	1
101 001100101	0000010000000	2	0010100010010	2	0100010000100	2	1000100010010	2
102 001100110	0000010000000	3	0010100010010	3	0100010000100	3	1000100010010	3
103 001100111	0000010000000	4	0010100010010	4	0100010000100	4	1000100010010	4
104 001101000	0000010000000	5	0010100010010	5	0100010000100	5	1000100010010	5
105 001101001	0000010000000	1	0010100010010	1	0100010000100	1	1000100010010	1
106 001101010	0000010000000	2	0010100010010	2	0100010000100	2	1000100010010	2
107 001101011	0000010000000	3	0010100010010	3	0100010000100	3	1000100010010	3
108 001101100	0000010000000	4	0010100010010	4	0100010000100	4	1000100010010	4
109 001101101	0000010000000	5	0010100010010	5	0100010000100	5	1000100010010	5
110 001101110	0000010000000	1	0010100010010	1	0100010000100	1	1000100010010	1
111 001101111	0000010000000	2	0010100010010	2	0100010000100	2	1000100010010	2
112 001110000	0000010000000	3	0010100010010	3	0100010000100	3	1000100010010	3
113 001110001	0000010000000	4	0010100010010	4	0100010000100	4	1000100010010	4
114 001110010	0000010000000	5	0010100010010	5	0100010000100	5	1000100010010	5
115 001110011	0000010000000	1	0010100010010	1	0100010000100	1	1000100010010	1
116 001110100	0000010000000	2	0010100010010	2	0100010000100	2	1000100010010	2
117 001110101	0000010000000	3	0010100010010	3	0100010000100	3	1000100010010	3
118 001110110	0000010000000	4	0010100010010	4	0100010000100	4	1000100010010	4
119 001110111	0000010000000	5	0010100010010	5	0100010000100	5	1000100010010	5
120 001111000	0000010000000	1	0010100010010	1	0100010000100	1	1000100010010	1
121 001111001	0000010000000	2	0010100010010	2	0100010000100	2	1000100010010	2
122 001111010	0000010000000	3	0010100010010	3	0100010000100	3	1000100010010	3
123 001111011	0000010000000	4	0010100010010	4	0100010000100	4	1000100010010	4
124 001111100	0000010000000	5	0010100010010	5	0100010000100	5	1000100010010	5
125 001111101	0000010000000	1	0010100010010	1	0100010000100	1	1000100010010	1
126 001111110	0000010000000	2	0010100010010	2	0100010000100	2	1000100010010	2
127 001111111	0000010000000	3	0010100010010	3	0100010000100	3	1000100010010	3





[illegible]

Data bits	Channel bits	state	Channel bits	state	Channel bits	state	Channel bits	state	
236	100000000	0000101010010	2	01001001000010	2	10101000000010	2	1000101010000	4
237	100000001	0000101010010	3	01010010000010	3	0100101010000	3	1010100000000	5
238	100000010	0000101010010	4	01010010000010	4	0100101010000	4	1010100000010	1
239	100000011	0000101010010	5	01010010000010	5	0100101010000	5	1010100000000	2
240	100000100	0000101010010	1	01010010000010	1	0100101000000	1	1001010010000	3
241	100000101	0000101010010	2	01010010000010	2	0100101000000	2	1001010010000	4
242	100000110	0000101010010	3	01010010000010	3	0100101000000	3	1001010010000	5
243	100000111	0000101010010	4	01010010000010	4	0100101000000	4	1010101010000	1
244	100001000	0000101010010	5	01010010000010	5	0100101000000	5	1010101010000	2
245	100001001	0001000000000	1	01010010100010	1	0101000010000	1	1010101010000	3
246	100001010	0001000000000	2	0101001010010	2	0101000010000	2	1010101010000	4
247	100001011	0001000000000	3	0101001010010	3	0101000010000	3	1010101010000	5
248	100001100	0001000000000	4	0101001010010	4	0101000010000	4	1010101010000	1
249	100001101	0001000000000	5	0101001010010	5	0101000010000	5	1001001010000	2
250	100001110	0001000000000	1	01010100000010	1	0001000000000	1	1001001010000	3
251	100001111	0001000000000	2	01010100000010	2	0101000000000	2	1001001010000	4
252	100010000	0001000000010	3	01010100000010	3	0101000000000	3	1001001010000	5
253	100010001	0001000000010	4	01010100000010	4	0101000000000	4	1000100010000	1
254	100010010	0001000000010	5	01010100000010	5	0101000000000	5	1010100010000	2
255	100010011	0001000000010	1	01010100000010	1	0101000000000	1	1000100010000	3
256	100010100	0001000000010	2	01010100000010	2	0101000000000	2	1000100010000	4
257	100010101	0001000000010	3	01010100000010	3	0101000000000	3	1000100010000	5
258	100010110	0001000000010	4	01010100000010	4	0101000000000	4	1000100010000	1
259	100010111	0001000000010	5	01010100000010	5	0101000000000	5	1000100010000	2
260	100011000	0001000000010	1	01010100000010	1	0101000000000	1	1000100010000	3
261	100011001	0001000000010	2	01010100000010	2	0101000000000	2	1000100010000	4
262	100011010	0001000000010	3	01010100000010	3	0101000000000	3	1000100010000	5
263	100011011	0001000000010	4	01010100000010	4	0101000000000	4	1000100010000	1
264	100011100	0001000000010	5	01010100000010	5	0101000000000	5	1000100010000	2
265	100011101	0001000000010	1	01010100000010	1	0101000000000	1	1000100010000	3
266	100011110	0001000000010	2	01010100000010	2	0101000000000	2	1000100010000	4
267	100011111	0001000000010	3	01010100000010	3	0101000000000	3	1000100010000	5
268	100011000	0001000000010	4	01010100000010	4	0101000000000	4	1000100010000	1
269	100011001	0001000000010	5	01010100000010	5	0101000000000	5	1000100010000	2
270	100011010	0001000000010	1	01010100000010	1	0001000000000	1	1001001010000	3
271	100011011	0001000000010	2	01010100000010	2	0101000000000	2	1001001010000	4
272	100010000	0001000000010	3	01010100000010	3	0101000000000	3	1001001010000	5
273	100010001	0001000000010	4	01010100000010	4	0101000000000	4	1000100010000	1
274	100010010	0001000000010	5	01010100000010	5	0101000000000	5	1010100010000	2
275	100010011	0001000000010	1	01010100000010	1	0001001010000	1	1010100010000	3
276	100010100	0001000000010	2	01010100000010	2	0101010010000	2	1010100010000	4
277	100010101	0001000000010	3	01010100000010	3	0101010010000	3	1010100010000	5
278	100010110	0001000000010	4	01010100000010	4	0101001010000	4	1001000010000	1
279	100010111	0001000000010	5	01010100000010	5	0101010010000	5	1001000010000	2
280	100011000	0001000000010	1	01010100000010	1	0100000000000	1	1010100010000	3
281	100011001	0001000000010	2	01010100000010	2	0100000000000	2	1010100010000	4
282	100011010	0001000000010	3	01010100000010	3	0100000000000	3	1010100010000	5
283	100011011	0001000000010	4	01010100000010	4	0100000000000	4	1000000010000	1
284	100011100	0001000000010	5	01010100000010	5	0100000000000	5	1000000010000	2
285	100011101	0001000000010	1	01010100000010	1	0100000000000	1	1000000010000	3
286	100011110	0001000000010	2	01010100000010	2	0101010010000	2	1000000010000	4
287	100011111	0001000000010	3	01010100000010	3	0101010010000	3	1000000010000	5
288	100100000	0001000000010	4	01010100000010	4	0100000000000	4	1000000010000	1
289	100100001	0001000000010	5	01010100000010	5	0100000000000	5	1000000010000	2
290	100100010	0001000000010	1	01010100000010	1	0101010010000	1	1000000010000	3
291	100100011	0001000000010	2	01010100000010	2	0101010010000	2	1000000010000	4
292	100100100	0001000000010	3	01010100000010	3	0101000000000	3	1000000010000	5
293	100100101	0001000000010	4	01010100000010	4	0101010010000	4	1001000010000	1
294	100100110	0001000000010	5	01010100000010	5	0101010010000	5	1001000010000	2
295	100100111	0001000000010	1	0001000010000	1	1000000000000	1	1001010010000	3
296	100101000	0001000000010	2	0001000010000	2	1000000000000	2	10101010000	4
297	100101001	0001000000010	3	0001000010000	3	1000000000000	3	100101010000	5
298	100101010	0001000000010	4	0001000010000	4	1000000000000	4	1010100010000	1
299	100101011	0001000000010	5	0001000010000	5	1000000000000	5	1010100010000	2
300	100101100	0001000000010	1	0100001010000	1	1000000000000	1	1010100010000	3
301	100101101	0001000000010	2	0100001010000	2	1000000000000	2	1010100010000	4
302	100101110	0001000000010	3	0100001010000	3	1000000000000	3	1010100010000	5
303	100101111	0001000000010	4	0100001010000	4	1000000000000	4	1000100010000	1
304	100110000	0001000000010	5	0100001010000	5	1000000000000	5	1000100010000	2
305	100110001	0001000000010	1	0101010010000	1	1001000000000	1	1000100010000	3
306	100110010	0001000000010	2	0101010010000	2	1001000000000	2	1000100010000	4
307	100110011	0001000000010	3	0101010010000	3	1001000000000	3	1000100010000	5
308	100110100	0001000000010	4	0101010010000	4	1001000000000	4	1000000010000	1
309	100110101	0001000000010	5	0101010010000	5	1001000000000	5	1010000010000	2
310	100110110	0001000000010	1	0101000000000	1	1000000000000	1	1010000010000	3
311	100110111	0001000000010	2	0100000000000	2	1000100000000	2	1010000010000	4
312	100111000	0001000000010	3	0100000000000	3	1000100000000	3	1010000010000	5
313	100111001	0001000000010	4	0100000000000	4	1000100000000	4	1010000010000	1
314	100111010	0001000000010	5	0100000000000	5	1000100000000	5	1010000010000	2
315	100111011	0001000000010	1	0100000000000	1	1001000000000	1	1010000010000	3
316	100111100	0001000000010	2	0100000000000	2	1001000000000	2	1010000010000	4
317	100111101	0001000000010	3	0100000000000	3	1010000000000	3	1010000010000	5
318	100111110	0001000000010	4	0100000000000	4	1010000000000	4	1000100000000	1
319	100111111	0001000000010	5	0100000000000	5	1000100000000	5	1000100000000	2

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FIG. 4F

Data bits	Channel bits	state Channel bits	state Channel bits	state Channel bits	state Channel bits	state
320 10100000	000100010100	1 001001001010	1 000101010000	1 100001000010	1 100100100000	3
321 10100001	000100010100	2 001001001010	2 000101010000	2 100001000010	2 100100100000	4
322 10100001	000100010100	3 001001001010	3 000101010000	3 100001000010	3 100100100000	5
323 10100001	000100010100	4 001001001010	4 000101010000	4 100001000010	4 100100100000	1
324 10100010	000100010100	5 001001001010	5 000101010000	5 100001000010	5 100100100000	2
325 10100010	000100010101	1 001001001010	1 000000100000	1 101000010010	1 100010100000	3
326 10100010	000100010101	2 001001001010	2 010000010000	2 101000010010	2 100010100000	4
327 10100011	000100010101	3 001001001010	3 010000010000	3 101000010010	3 100010100000	5
328 10100000	000100010101	4 001001001010	4 010000010000	4 101000010010	4 101010100000	1
329 10100001	000100010101	5 001001001010	5 010000010000	5 101000010010	5 101010100000	2
330 10100010	000100100000	1 010010001010	1 010100100000	1 100100001010	1 101010100000	3
331 10100011	000100100000	2 010010001010	2 010100100000	2 100100001010	2 101010100000	4
332 10100100	000100100000	3 010010001010	3 010100100000	3 100100001010	3 101010100000	5
333 10100101	000100100000	4 010010001010	4 010100100000	4 100100001010	4 101000100000	1
334 10100110	000100100000	5 010010001010	5 010100100000	5 100100001010	5 101000100000	2
335 10100111	000100100001	1 000101010010	1 010010100000	1 100001000010	1 101000100000	3
336 10101000	000100100001	2 000101010010	2 010010100000	2 100001000010	2 101000100000	4
337 10101001	000100100001	3 000101010010	3 010010100000	3 100001000010	3 101000100000	5
338 10101001	000100100001	4 000101010010	4 010010100000	4 100001000010	4 100001000000	1
339 10101001	000100100001	5 000101010010	5 010010100000	5 100001000010	5 100001000000	2
340 10101000	000100100010	1 010010010010	1 001000100000	1 101000100010	1 100000100000	3
341 10101001	000100100010	2 010010010010	2 001000100000	2 101000100010	2 100000100000	4
342 10101010	000100100010	3 010010010010	3 001000100000	3 101000100010	3 100000100000	5
343 10101011	000100100010	4 010010010010	4 001000100000	4 101000100010	4 101001000000	1
344 10101000	000100100010	5 010010010010	5 001000100000	5 101000100010	5 101001000000	2
345 10101001	000100100100	1 010000000010	1 010000100000	1 100100010010	1 101001000000	3
346 10101010	000100100100	2 010000000010	2 010000100000	2 100100010010	2 101001000000	4
347 10101011	000100100100	3 010000000010	3 010000100000	3 100100010010	3 101001000000	5
348 10101100	000100100100	4 010000000010	4 010000100000	4 100100010010	4 100001000000	1
349 10101101	000100100100	5 010000000010	5 010000100000	5 100100010010	5 100001000000	2
350 10101110	000100100101	1 001001010010	1 001001010000	1 100010010010	1 100001000000	3
351 10101111	000100100101	2 001001010010	2 001001010000	2 100010010010	2 100001000000	4
352 10110000	000100100101	3 001001010010	3 001001010000	3 100010010010	3 100001000000	5
353 10110001	000100100101	4 001001010010	4 001001010000	4 100010010010	4 100101000000	1
354 10110010	000100100101	5 001001010010	5 001001010000	5 100010010010	5 100101000000	2
355 10110011	000100100100	1 010010100010	1 001001000000	1 101000101010	1 100101000000	3
356 10110010	000100100100	2 010010100010	2 001001000000	2 101000101010	2 100101000000	4
357 10110010	000100100100	3 010010100010	3 001001000000	3 101000101010	3 100101000000	5
358 10110010	000100101000	4 010010100010	4 001001000000	4 101000101010	4 100010000000	1
359 10110011	000100101000	5 010010100010	5 001001000000	5 101000101010	5 100010000000	2
360 10110100	000100101001	1 001001000010	1 010001000000	1 100000010010	1 100010000000	3
361 10110101	000100101001	2 001001000010	2 010001000000	2 100000010010	2 100010000000	4
362 10110110	000100101001	3 001001000010	3 010001000000	3 100000010010	3 100010000000	5
363 10110111	000100101001	4 001001000010	4 010001000000	4 100000010010	4 101010000000	1
364 10110100	000100101010	5 001001000010	5 010001000000	5 100000010010	5 101010000000	2
365 10110101	000100101010	1 010000010010	1 010000010000	1 101000010010	1 101010000000	3
366 10110110	000100101010	2 010000010010	2 010000010000	2 101000010010	2 101010000000	4
367 10110111	000100101010	3 010000010010	3 010000010000	3 101000010010	3 101010000000	5
368 10110000	000100101010	4 010000010010	4 010000010000	4 101000010010	4 100100000000	1
369 10110001	000100101010	5 010000010010	5 010000010000	5 101000010010	5 100100000000	2
370 10110010	000100100000	1 010010101010	1 010010000000	1 100100100010	1 100100000000	3
371 10110011	000100100000	2 010010101010	2 010010000000	2 100100100010	2 100100000000	4
372 10110100	000100100000	3 010010101010	3 010010000000	3 100100100010	3 100100000000	5
373 10110101	000100100000	4 010010101010	4 010010000000	4 100100100010	4 100000000000	1
374 10110110	000100100000	5 010010101010	5 010010000000	5 100100100010	5 100000000000	2
375 10110111	000100100001	1 000101000100	1 001010000000	1 100010010010	1 101000000000	3
376 10111000	000100100001	2 000101000100	2 001010000000	2 100010010010	2 101000000000	4
377 10111001	000100100001	3 000101000100	3 001010000000	3 100010010010	3 101000000000	5
378 10111010	000100100001	4 000101000100	4 001010000000	4 100010010010	4 100100000000	1
379 10111011	000100100001	5 000101000100	5 001010000000	5 100010010010	5 100100000000	2
380 10111100	000000000010	1 000100100001	1 010000000000	1 100000000001	1 100100000000	3
381 10111101	000000000010	2 000100100001	2 010000000000	2 100000000001	2 100100000000	4
382 10111110	000000000010	3 000100100001	3 010000000000	3 100000000001	3 100100000000	5
383 10111111	000000000010	4 000100100001	4 010000000000	4 100000000001	4 100100000000	1





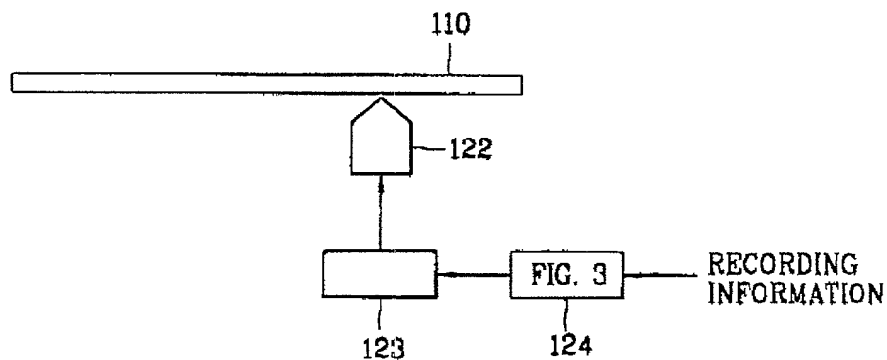


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FIG. 5

INFORMATION WORDS (DECIMAL NOTATION)	STATE	CODE WORDS	NEXT STATE
000000001 (1)	S1	0000000000100	S2
000000011 (3)	S2	0001010001010	S4
000000101 (5)	S4	0101001001001	S1
000001100 (12)	S1	0000000001010	S3
000010011 (19)	S3	0101000010100	S5

FIG. 6



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FIG. 7

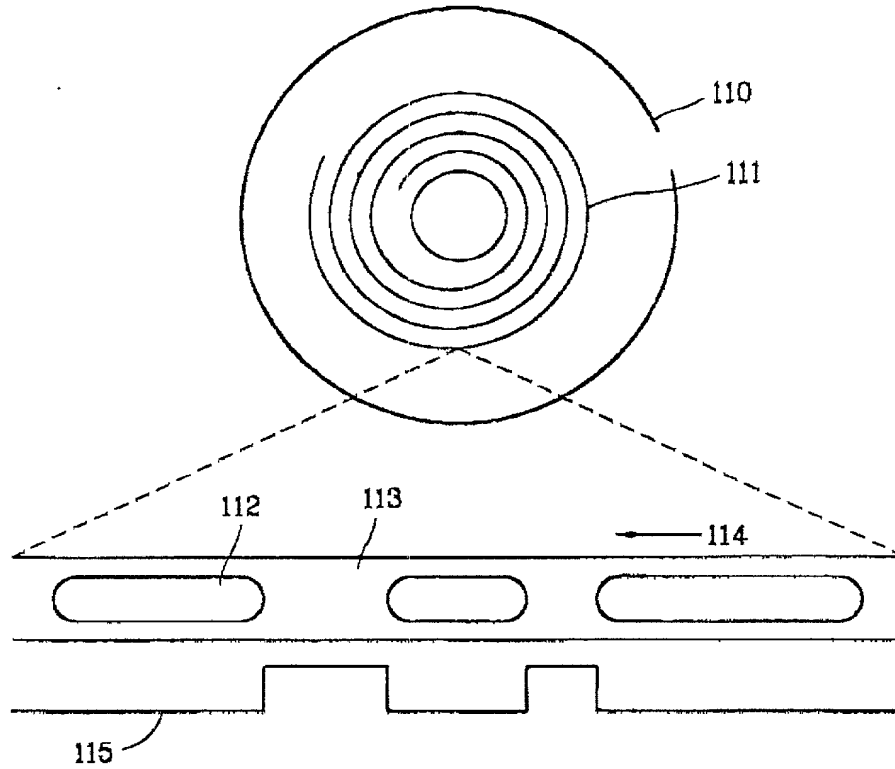


FIG. 8



FIG. 9

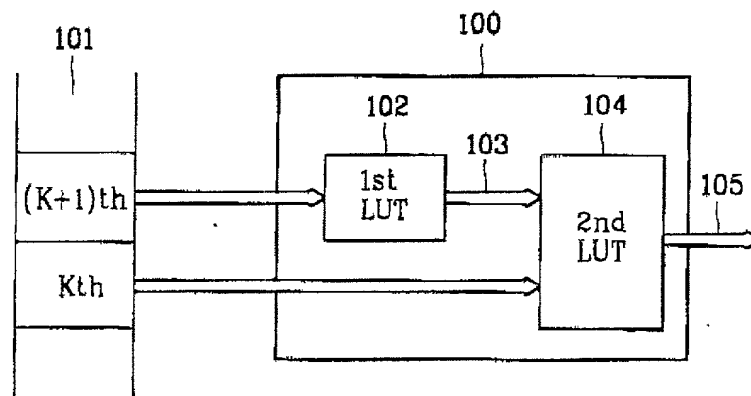


FIG. 10

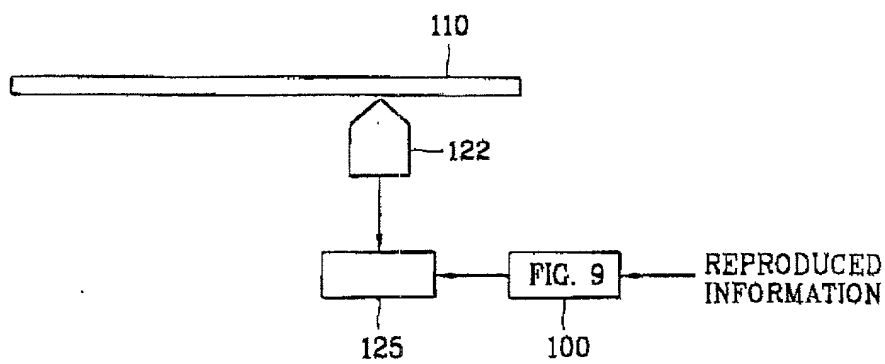


FIG. 11

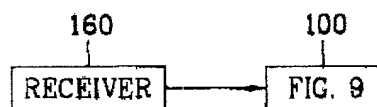


FIG. 12

SUBGROUP	1st KIND								2nd KIND				
	STATE 1	STATE 2	STATE 3	STATE 4	STATE 5	STATE 6	STATE 7	STATE 8	STATE 9	STATE 10	STATE 11	STATE 12	STATE 13
E00	24	32	32	32	32	24	32	20	0	0	0	0	0
E01	25	12	12	12	12	25	12	33	0	0	0	0	0
E10	0	0	0	0	0	0	0	0	24	24	24	32	39
E11	0	0	0	0	0	0	0	0	25	25	25	12	2

FIG. 13A

[illegible]



FIG. 13C

Data Channel bits state Channel bits state Channel bits state Channel bits state Channel bits state Channel bits state Channel bits state Channel bits state Channel bits state									
481	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
482	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
483	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
484	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
485	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
486	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
487	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
488	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
489	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
490	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
491	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
492	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
493	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
494	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
495	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
496	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
497	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
498	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
499	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
500	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
501	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
502	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
503	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
504	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
505	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
506	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
507	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
508	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
509	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
510	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001
511	0000101000001	6	0001001010001	7	0010001010001	7	0010001010001	7	0010001010001



FIG. 14

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SUBGROUP	1st KIND							2nd KIND						
	STATE 1	STATE 2	STATE 3	STATE 4	STATE 5	STATE 6	STATE 7	STATE 8	STATE 9	STATE 10	STATE 11	STATE 12	STATE 13	
E00	114	114	114	114	113	113	114	114	0	0	0	0	0	
E01	71	71	71	71	72	72	71	71	0	0	0	0	0	
E10	0	0	0	0	0	0	0	0	112	113	112	112	112	
E11	0	0	0	0	0	0	0	0	75	74	75	75	75	

FIG. 15A

[illegible]

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89</											

FIG. 15C

[illegible]

	1st KIND			2nd KIND	
SUBGROUP	STATE 1	STATE 2	STATE 3	STATE 4	STATE 5
E00	1176	1176	1176	0	0
E01	771	771	771	0	0
E10	0	0	0	1169	1169
E11	0	0	0	782	782

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FIG. 17A

	State 1	State 2	State 3	State 4	State 5
Data	Channel bits	state Channel bits	state Channel bits	state Channel bits	state Channel bits
0	0000000000000000	1 0010000000000000	1 0100000000000000	1 1000000000000000	1 1001000000000000
1	0000000000000001	2 0010000000000001	2 0100000000000001	2 1000000000000001	2 1001000000000001
2	0000000000000010	3 0010000000000010	3 0100000000000010	3 1000000000000010	3 1001000000000010
3	0000000000000011	4 0010000000000011	4 0100000000000011	4 1000000000000011	4 1001000000000011
4	0000000000000100	5 0010000000000100	5 0100000000000100	5 1000000000000100	5 1001000000000100
5	0000000000000101	1 0010000000000101	3 0100000000000101	3 1000000000000101	3 1001000000000101
6	0000000000000110	2 0010000000000110	4 0100000000000110	4 1000000000000110	4 1001000000000110
7	0000000000000111	3 0010000000000111	5 0100000000000111	5 1000000000000111	5 1001000000000111
8	0000000000001000	1 0010000000001000	1 0100000000001000	1 1000000000001000	1 1001000000001000
9	0000000000001001	2 0010000000001001	2 0100000000001001	2 1000000000001001	2 1001000000001001
10	0000000000001010	3 0010000000001010	3 0100000000001010	3 1000000000001010	3 1001000000001010
11	0000000000001011	4 0010000000001011	4 0100000000001011	4 1000000000001011	4 1001000000001011
12	0000000000001100	5 0010000000001100	5 0100000000001100	5 1000000000001100	5 1001000000001100
13	0000000000001101	1 0010000000001101	1 0100000000001101	1 1000000000001101	1 1001000000001101
14	0000000000001110	2 0010000000001110	2 0100000000001110	2 1000000000001110	2 1001000000001110
15	0000000000001111	3 0010000000001111	3 0100000000001111	3 1000000000001111	3 1001000000001111
16	0000000000010000	1 0010000000010000	1 0100000000010000	1 1000000000010000	1 1001000000010000
17	0000000000010001	2 0010000000010001	2 0100000000010001	2 1000000000010001	2 1001000000010001
18	0000000000010010	3 0010000000010010	3 0100000000010010	3 1000000000010010	3 1001000000010010
19	0000000000010011	4 0010000000010011	4 0100000000010011	4 1000000000010011	4 1001000000010011
20	0000000000010100	5 0010000000010100	5 0100000000010100	5 1000000000010100	5 1001000000010100
21	0000000000010101	1 0010000000010101	1 0100000000010101	1 1000000000010101	1 1001000000010101
22	0000000000010110	2 0010000000010110	2 0100000000010110	2 1000000000010110	2 1001000000010110
23	0000000000010111	3 0010000000010111	3 0100000000010111	3 1000000000010111	3 1001000000010111
24	0000000000011000	4 0010000000011000	4 0100000000011000	4 1000000000011000	4 1001000000011000
25	0000000000011001	5 0010000000011001	5 0100000000011001	5 1000000000011001	5 1001000000011001
26	0000000000011010	1 0010000000011010	1 0100000000011010	1 1000000000011010	1 1001000000011010
27	0000000000011011	2 0010000000011011	2 0100000000011011	2 1000000000011011	2 1001000000011011
28	0000000000011100	3 0010000000011100	3 0100000000011100	3 1000000000011100	3 1001000000011100
29	0000000000011101	4 0010000000011101	4 0100000000011101	4 1000000000011101	4 1001000000011101
30	0000000000011110	5 0010000000011110	5 0100000000011110	5 1000000000011110	5 1001000000011110
31	0000000000011111	1 0010000000011111	1 0100000000011111	1 1000000000011111	1 1001000000011111
32	0000000000010000	2 0010000000010000	2 0100000000010000	2 1000000000010000	2 1001000000010000
33	0000000000010001	3 0010000000010001	3 0100000000010001	3 1000000000010001	3 1001000000010001
34	0000000000010010	4 0010000000010010	4 0100000000010010	4 1000000000010010	4 1001000000010010
35	0000000000010011	5 0010000000010011	5 0100000000010011	5 1000000000010011	5 1001000000010011
36	0000000000010100	1 0010000000010100	1 0100000000010100	1 1000000000010100	1 1001000000010100
37	0000000000010101	2 0010000000010101	2 0100000000010101	2 1000000000010101	2 1001000000010101
38	0000000000010110	3 0010000000010110	3 0100000000010110	3 1000000000010110	3 1001000000010110
39	0000000000010111	4 0010000000010111	4 0100000000010111	4 1000000000010111	4 1001000000010111
40	0000000000011000	5 0010000000011000	5 0100000000011000	5 1000000000011000	5 1001000000011000
41	0000000000011001	1 0010000000011001	1 0100000000011001	1 1000000000011001	1 1001000000011001
42	0000000000011010	2 0010000000011010	2 0100000000011010	2 1000000000011010	2 1001000000011010
43	0000000000011011	3 0010000000011011	3 0100000000011011	3 1000000000011011	3 1001000000011011
44	0000000000011100	4 0010000000011100	4 0100000000011100	4 1000000000011100	4 1001000000011100
45	0000000000011101	5 0010000000011101	5 0100000000011101	5 1000000000011101	5 1001000000011101

FIG. 17A



[illegible]



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Attorney Docket No. 630-1167P

### COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT AND DESIGN APPLICATIONS

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title:

METHOD AND APPARATUS FOR CODING INFORMATION, METHOD AND APPARATUS FOR DECODING INFORMATION,  
METHOD OF FABRICATING A RECORDING MEDIUM, THE RECORDING MEDIUM AND MODULATED SIGNAL.

In Appropriate  
Information -  
Use Without  
Specification  
Checked:

the specification of which is attached hereto. If not attached hereto,

the specification was filed on \_\_\_\_\_ as  
United States Application Number \_\_\_\_\_  
and amended on \_\_\_\_\_ (if applicable) and/or  
the specification was filed on \_\_\_\_\_ as PCT  
International Application Number \_\_\_\_\_; and was  
amended under PCT Article 19 on \_\_\_\_\_ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representative or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

#### Prior Foreign Application(s)

#### Priority Claimed

Part Priority  
Information:  
Appropriate)

99203739.0 (Number)	EPO (Country)	November 11, 1999 (Month/Day/Year Filed)	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Month/Day/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Month/Day/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Month/Day/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional applications(s) listed below.

Part Provisional  
Application(s):  
(any)

_____ (Application Number)	_____ (Filing Date)
_____ (Application Number)	_____ (Filing Date)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More than 12 Months (6 Months for Designs) Prior to the Filing Date of This Application:

Part Requested  
Information:  
Appropriate)

Country	Application Number	Date of Filing (Month/Day/Year)
_____	_____	_____
_____	_____	_____

I hereby claim the benefit under Title 35, United States Code, §120 of any United States and/or PCT application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States and/or PCT application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Part Prior U.S.  
Application(s):  
(any)

_____ (Application Number)	_____ (Filing Date)	_____ (Status - patented, pending, abandoned)
_____ (Application Number)	_____ (Filing Date)	_____ (Status - patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the attorneys identified below, unless the inventor(s) or assignee provides said attorneys with a written notice to the contrary:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

GIVEN NAME/FAMILY NAME		INVENTOR'S SIGNATURE	DATE*
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Residence (City, State & Country)		CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME/FAMILY NAME		INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME/FAMILY NAME		INVENTOR'S SIGNATURE	DATE*
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MAILING ADDRESS (Complete Street Address including City, State & Country)			

\*DATE OF SIGNATURE